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09/777,202	02/02/2001	Brian William Hughes	10004543-1	3035

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 05/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/777,202	HUGHES, BRIAN WILLIAM	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/21/2005 has been entered.

This is a Non-Final Office Action in response to Amendment and RCE filed 3/21/2005, in reply to the Final Office Action dated 9/30/2004.

Claims 1, 5, 9, 13, 16 and 20 have been amended.

Claims 1-20 are pending and presently under examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hedberg et al. (U.S. Patent No. 6,026,505) in view of Conan (U.S. Patent No. 5,504,712).

Regarding independent Claims 1, 9, Hedberg substantially discloses a method and a system for eliminating faulty memory cells of memory array (A) on a semiconductor chip (10) by replacing the faulty cells with redundant column and row lines using an array built in self testing (ABIST), Figures 1 and 2, comprising:

Determining, using a memory cell tester [array built in self testing (ABIST)], if the cells in column group (C0 to Cn) of the memory array (A) are defective or non operational, herewith "defective", by performing self testing on the memory array A, and applying the test results (pass/fail signal) to a two dimension failed address register 33 which also receives column and row addresses of the cells of the array A (col. 3, lines 1-50), and also described in the Disclosure of the Invention of the Invention, (col. 2, lines 1-22).

Configuring the faulty cells in the column group (C1 to Cn), using a column group reconfigurer (redundancy implementation processor 35), which substitutes appropriate redundant column lines for faulty array column group (C1 to Cn), for example by replacing column C1 with the redundant spare column line RC1, for example with column C1 having 3 failed cells identified by an X, which is greater than a predetermined number 2, as disclosed, "if the column fail count along any column is greater than 2, as set by the available number of row redundant lines, the column count is set and the column address is stored or saved" Figures 2, 3 and 6.

Identifying by row the remaining defective cells, using (ABIST), Figure 1, which identifies remaining defective cells in the memory array, which were not previously replaced by the redundant spare column line RC1, by "further testing the array either along rows or columns to identify any additional faulty cells while masking the cells having the stored column addresses and storing the row addresses having the faulty cells in second registers until all of the second registers store row addresses", as described in the Disclosure of the Invention of the Invention, (col. 2, lines 1-22).

Configuring the rows of the memory array, using a row reconfigurer, such as a redundancy implementation processor 35, which substitutes appropriate redundant row lines for faulty array raw of the memory array, Figure 4, by identifying faulty or failed cells in two of the array row lines R0 to Rm of Figure 2 which can be replaced by the two redundant row lines RR1 and RR2 or can indicate that both of the redundant row lines RR1 and RR2 are to be used to replace two of the faulty array row lines R0 to Rm. (see column 5, lines 62-67, Figure 4).

Hedberg does not explicitly disclose, "configuring column groups of the memory array to replace ones of the column groups, ...with spare column groups by using bit line multiplexers to shift in a replacement column group of memory cells into the array".

However, in analogous art, Conan (U.S. Patent No. 5,504,712) discloses, Figures 1-4, a memory organized in column groups (GOa, Gob) of p columns of memory cells in a main network, and column groups (CR0a, CR0b) of r redundancy columns, in sets E0, E1, . . ., each group (CR0a) of redundancy columns corresponding to a group (G0a) of columns of memory cells of the main network.

Further, Conan discloses selecting redundancy columns to replace defective columns, using selection circuit CSR capable of defining one among r redundancy columns, simultaneously for all the groups of r columns of all the sets. Each of the groups of redundancy columns is associated with an amplifier and is connected to this amplifier by means of a multiplexer in the same way as the columns of memory cells of the main network are connected to the amplifiers by means of a multiplexer. A decoder DC controls the linking of the columns of the main network, and the redundant column selection circuit CSR controls the linking of the redundant columns, see description with respect to Figure 4.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement multiplexers as taught by Conan in the redundancy allocation method of Hedberg for the purpose of replacing defective cells with good cells by selecting groups of redundancy columns, using multiplexers, in lieu of a laser fuse blowing device. The incorporation of Conan in the method of Hedberg achieves increasing the possibilities of redundancy without increasing the amount of space occupied in the immediate vicinity of the columns of the memory. In particular, the size of the multiplexer, which, under the control of the circuit CSR, designates one among r columns, is reduced to the minimum and the additional, added-on elements, such as the additional memory zones of the register, are shifted towards the periphery (Col. 8, lines 28-36).

Regarding Claims 2, 3, 10, 11, Hedberg discloses testing memory cells as shown in flow chart (Figure 6), including the steps of a screen test for finding hard faulty cell

located along the column group (C1 to Cn) of the memory array (A), including (counter 38) Figure 7, which counts the number of the defective cells identified in each of the column stored in the column fail address register circuit (22). If the column fail count, along any column, is greater than a threshold count (2), as set by the available number of row redundant lines, then the column count is set and the column address is stored or saved. If the column fail count is not greater than 2, then the column under test is incremented (column 13, lines 30-54).

Regarding Claims 4, 12, Hedberg discloses determining if cells in each column group (C1 to Cn) of the memory array (A) are defective, comprising: generating a memory address using address counter 27, which generate the test data and address data, respectively, for the self-testing of the memory array (A) through the multiplexer 11. The test data is written into cells of the array A of the memory chip 10 and then read out to a data compression unit 31, where it is compared with a duplicate of the test data written into the cells of the array of the memory chip 10 from the data pattern generator 29. The results of the comparison are reduced to a single pass/fail or fault/no fault signal (column 3, line 4-13).

Regarding Claims 5-7,13-14, Hedberg discloses configuring the columns and rows of the memory array (A) FIGS. 1 and 2, using redundancy implementation processor 35 which substitutes appropriate redundant column or row lines for faulty array column or row lines. The address information stored in the two dimension failed address register (FIGS. 1, 3 and 4) is serially read out to the SCAN OUT terminal and then applied to the redundancy implementation processor 35 for substituting redundant

column and row lines for the identified failed array column and row lines. Testing the memory array after performing the configuring column groups, using array built in self testing (ABIST) formed on the semiconductor chip (10) having an array of memory cells (A).

Regarding Claims 8 and 15 Hedberg discloses configuring column groups and configuring rows, which are performed by built-in self repair (BISR), such as processor 35, which includes a laser-fuse blowing device or an electrical latch setting circuit.

Regarding independent Claim 16, Hedberg substantially discloses a method of eliminating faulty memory cells of memory array (A) on a semiconductor chip (10) by replacing the faulty cells with redundant column and row lines using an array built in self testing (ABIST), Figures 1 and 2, comprising:

Determining if the cells in each row of the memory array (A) are operational (good cells) by performing self testing on the memory array A, and applying the test results (pass/fail signal) to a two dimension failed address register 33 which also receives column and row addresses of the cells of the array A (col. 3, lines 1-50), and, also, described in the Disclosure of the Invention of the Invention, (col. 2, lines 1-22)

Configuring the rows of the memory array (A), using a row reconfigurer, such as a redundancy implementation processor 35, which substitutes appropriate redundant row lines for faulty array raw of the memory array, Figure 4, by identifying faulty or failed cells in two of the array row lines R0 to Rm of Figure 2 which can be replaced by the two redundant row lines RR1 and RR2 or can indicate that both of the redundant

row lines RR1 and RR2 are to be used to replace two of the faulty array row lines R0 to Rm. The failed row included a predetermined number of non operational cells, which are designated by X in Figure 2, with spare rows corresponding to a row count 2 (see column 5, lines 62-67, Figure 4).

Identifying by row the remaining defective cells, using (ABIST), Figure 1, which identifies remaining defective cells in the memory array, which were not previously replaced by the redundant spare row redundant row lines RR1 and RR2, by "further testing the array either along rows or columns to identify any additional faulty cells while masking the cells having the stored column addresses and storing the row addresses having the faulty cells in second registers until all of the second registers store row addresses", as described in the Disclosure of the Invention of the Invention, (col. 2, lines 1-22).

Configuring the faulty cells in the column group (C1 to Cn), using a column group reconfigurer (redundancy implementation processor 35), which substitutes appropriate redundant column lines for faulty array column group (C1 to Cn), for example by replacing column C1 with the redundant spare column line RC1, for example with column C1 having 3 failed cells identified by an X, which is greater than a predetermined number 2, as disclosed, "if the column fail count along any column is greater than 2, as set by the available number of row redundant lines, the column count is set and the column address is stored or saved" Figures 2, 3 and 6.

Hedberg does not explicitly disclose, "activating an alternate word line to shift in a replacement row of memory cells into the memory array".

However, in analogous art, Conan (U.S. Patent No. 5,504,712) discloses, Figures 1-4, a memory organized in column groups (GOa, Gob) of p columns of memory cells in a main network, and column groups (CR0a, CR0b) of r redundancy columns, in sets E0, E1, . . ., each group (CR0a) of redundancy columns corresponding to a group (G0a) of columns of memory cells of the main network, further including, selecting redundancy columns to replace defective columns, using selection circuit CSR for controlling a multiplexer for linking the redundant columns associated with an amplifier, Figure 4.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement multiplexers as taught by Conan in the redundancy allocation method of Hedberg for the purpose of replacing defective cells with good cells by selecting groups of redundancy rows, using multiplexers, in lieu of a laser fuse blowing device. The incorporation of Conan in the method of Hedberg achieves increasing the possibilities of redundancy without increasing the amount of space occupied in the immediate vicinity of the columns of the memory. In particular, the size of the multiplexer, which, under the control of the circuit CSR, designates one among r columns, is reduced to the minimum and the additional, added-on elements, such as the additional memory zones of the register, are shifted towards the periphery (Col. 8, lines 28-36).

Regarding Claims 17, 18, Hedberg discloses testing memory cells as shown in flow chart (FIG. 6), including the steps of a screen test for finding hard faulty cell located along the row. A (counter 38) Figure 7 counts the number of the defective

cells identified in each of the column stored in the column fail address register circuit (22). After the last column has been tested, the cells are again tested with additional test pulses using more complex test patterns, until a failed cell has been detected. If the failed cell did not have a previously assigned address row or column and the row count is not equal to 2, the row count is incremented and the row address is saved. If the row count is equal to 2 and the column count is not equal to 1, the column count is incremented and the column address is stored or saved, and further testing of the cells continues (column 13, lines 30-54).

Regarding Claim 19, Hedberg discloses determining if cells in each row (R0 to Rm) of Figure 2 are operational (good), comprising: generating at memory address using address counter 27, which generate the test data and address data, respectively, for the self-testing of the memory array (A) through the multiplexer 11. The test data is written into cells of the array A of the memory chip 10 and then read out to a data compression unit 31, where it is compared with a duplicate of the test data written into the cells of the array of the memory chip 10 from the data pattern generator 29. The results of the comparison are reduced to a single pass/fail or fault/no fault signal (column 3, line 4-13).

Regarding Claim 20, Hedberg discloses configuring the columns and rows of the memory array (A) FIGS. 1 and 2, using redundancy implementation processor 35 which substitutes appropriate redundant column or row lines for faulty array column or row lines. The address information stored in the two dimension failed address register (FIGS. 1, 3 and 4) is serially read out to the SCAN OUT terminal and then applied to

the redundancy implementation processor 35 for substituting redundant column and row lines for the identified failed array column and row lines. Testing the memory array after performing the configuring column groups, using array built in self testing (ABIST) formed on the semiconductor chip (10) having an array of memory cells (A).

Response to Arguments

Applicant's arguments with respect to claims 1-120 have been considered but are moot in view of the new grounds of rejection.

Regarding independent Claims 1 and 9, as amended, in response to Applicant's argument, Examiner agrees that the prior art by Hedberg and Proebsting taken alone or in combination does not describe bit line multiplexers to shift in a replacement column group of memory cells into the array.

However, under the new grounds of rejection, in an analogous art, Conan (U.S. Patent No. 5,504,712) discloses, Figures 1-4, a memory organized in column groups (GOa, Gob) of p columns of memory cells in a main network, and column groups (CR0a, CR0b) of r redundancy columns, in sets E0, E1, . . ., each group (CR0a) of redundancy columns corresponding to a group (G0a) of columns of memory cells of the main network, including bit line multiplexers for shifting in a replacement column group (CR0a, CR0b) of memory cells into the array, as described in the present Office Action above. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the bit line multiplexers of Conan in the

device of Hedberg, for the same obvious and motivational reasons described in claim 1 and 9 above.

Regarding independent Claim 16, as amended, in response to Applicant's argument, Examiner agrees that the prior art by Hedberg and Proebsting taken alone or in combination does not describe, "activating an alternate word line to shift in a replacement row of memory cells into the memory array".

However, under the new grounds of rejection, in an analogous art, Conan (U.S. Patent No. 5,504,712) discloses, Figures 1-4, a memory organized in column groups (GOa, Gob) of p columns of memory cells in a main network, and column groups (CR0a, CR0b) of r redundancy columns, in sets E0, E1, . . ., each group (CR0a) of redundancy columns corresponding to a group (G0a) of columns of memory cells of the main network, further including, selecting redundancy columns to replace defective columns, using selection circuit CSR for controlling a multiplexer for linking the redundant columns associated with an amplifier, Figure 4. Thus, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the bit line multiplexers of Conan in the device of Hedberg, for the same obvious and motivational reasons described in claim 1 and 9 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2133

By: 5/13/05

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